CONTROL OF A PHOTOSENSITIVE CELL

Background Of The Invention

1. Field of the Invention

The present invention relates to the control of a photosensitive cell of an image sensor for use in shooting devices such as, for example, video cameras or digital photographic devices. More specifically, the present invention relates to a semiconductor monolithic photosensitive cell.

2. Discussion of the Related Art

Fig. 1 schematically illustrates the circuit of a photosensitive cell of an array of photosensitive cells distributed in rows and columns of an image sensor. To each photosensitive cell of the array are associated a reset device and a read device. The reset device is formed of an N-channel MOS transistor M_1, interposed between a supply rail Vdd and a read node S. The gate of reset transistor M_1 is capable of receiving a reset control signal RST. Read node S is capable of storing charges. For this purpose, a diode formed by a separate component may be connected to node S. The capacitance of node S may also correspond to the capacitances of the sources of transistors M_1 and M_4, to the input capacitance of transistor M_2, and to all the stray capacitances present at node S.

The read device is formed of the series connection of first and second N-channel MOS transistors M_2, M_3. The drain of the first read transistor M_2 is connected to supply rail Vdd. The source of the second read transistor M_3 is connected to an output terminal P. The gate of first read transistor M_2 is connected to read node S. The gate of second read transistor M_3 is capable of receiving a read signal RD. The relative position of read transistors M_2 and M_3 may be inverted without substantially modifying the device operation.

The photosensitive cell comprises a photodiode D having its anode connected to a reference supply rail or circuit ground GND and its cathode connected to read node S via an N-channel MOS transfer transistor M_4. The gate of transfer transistor M_4 is capable of receiving a transfer control signal T_X. Generally, signals RD, RST, and T_X are

provided by control circuits, not shown in Fig. 1, and may be simultaneously provided to all the photosensitive cells of the same row of the cell array. Output terminals P of the photosensitive cells of the same column are connected to a processing circuit (not shown).

Fig. 2 shows an example of a timing diagram of signals RD, RST, T_X of voltage V_S between read node S and the circuit ground, and of voltage V_D across photodiode D of the circuit of Fig. 1 between two read cycles of the photosensitive cell. Signals RD, RST, and T_X are binary signals varying between high and low levels that can be different for each of the signals.

Duration T_{RD} corresponds to the duration of a read cycle. At the beginning of a read cycle, a given amount of charges (electrons) is stored at the level of photodiode D. The read cycle starts when signal RD switches high, which corresponds to the selection of the array row containing the photosensitive cell to be read. Signal RST is then high. Reset transistor M_1 is thus on. Voltage V_S is then substantially equal to voltage Vdd. Signal RST is then set to the low state. Reset transistor M_1 is then off. Voltage V_S at read node S is then set to a reset level V_{RST} that can be lower than voltage Vdd due to a coupling with reset transistor M_1. Reset level V_{RST} is generally disturbed by noise essentially coming from the thermal noise of the channel of reset transistor M_1. This noise is sampled and maintained on the read node upon blocking of reset transistor M_1. Reset level V_{RST} is then stored outside the photosensitive cell via read transistors M_2, M_3.

Control signal T_X is then set to the high state. Transfer transistor M_4 is thus on, which enables transfer of the charges stored in photodiode D to read node S. Photodiode D is designed so that all the charges stored therein are transferred to read node S. Voltage V_S then decreases to a useful signal level V_U. Signal T_X is then set back to the low level. Photodiode D is thus isolated again and, due to the lighting, charges are stored again. Useful signal level V_U at read node S is then read via read transistors M_2, M_3. Like reset level V_{RST}, useful signal level V_U is disturbed, in particular, by the thermal noise of the channel of reset transistor M_1 which has been sampled and maintained on

the read node. The subtraction of signals V_U and V_{RST} by the processing circuit enables suppressing the noise of reset transistor M_1 by a double correlated sampling. Signal RST is then set to the high level. Voltage V_S at read node S is then maintained equal to voltage Vdd. The read cycle ends when signal RD is set to the low state to deselect the photosensitive cell.

Duration T_{FR} between the beginning of two read cycles of the same row of photosensitive cells corresponds to the duration or period of an image sensor frame. Duration T_{IRD} between the end of a read cycle of a cell row and the beginning of the next read cycle of the same cell row may be such that under too strong a lighting, a saturation of the photodiode may occur. It is thus preferable to limit duration T_{INT} of the integration phase during which charges are formed and stored at the level of each photodiode D.

For this purpose, an example of a conventional control consists of maintaining reset control signal RST high for the entire duration T_{IRD} between two read cycles of the same row. Transfer control signal T_X is set to the high level little after the end of a read cycle. Photodiode D then permanently discharges towards the supply rail. Signal T_X is set to the low state at the end of a duration T_{RST} after the end of the read cycle, to start an integration phase.

For technologies of increasing density with photosensitive cells of small dimensions and control signals that become smaller and smaller, it becomes difficult to ensure proper transfer of charges from photodiode D to read node S during a read cycle or before the beginning of an integration phase.

To improve the charge transfer, the high level of signal T_X applied on the gate of transfer transistor M_4 is increased to increase the intensity of the electric field enabling flowing of the charges. However, if this level becomes too high, a potential well is created in the channel of transfer transistor M_4 of a value greater than reset voltage V_{RST}. Charges can then be stored during the charge transfer to the channel region of transfer transistor M_4. Part of these charges can then be sent back to photodiode D at the falling edge of signal T_X from the high level to the low level.

When the photosensitive cell is submitted to a low lighting, the charge return risk appears to be stronger with such an implementation when transfer signal T_X is set to the low state before the beginning of an integration phase than during a read cycle. This may translate as a charge injection from read node S to the photodiode before the integration phase and may result in an offset of the signal subsequently measured in the absence of light, with an increase of non-uniformities at a low signal level.

Summary Of The Invention

The present invention provides a method and a device for controlling a photosensitive cell enabling improvement of the complete transfer of the photodiode charges to the read node before the beginning of an integration phase of the photodiode.

The present invention provides a method for controlling a photosensitive cell comprising a photodiode connected to a read node via a MOS transfer transistor, the read node being connected to a source of a reference voltage via a MOS reset transistor, cyclically comprising a waiting phase of non-zero duration at the end of which the photodiode is isolated from the reference voltage; an integration phase during which the voltage of the photodiode varies from a reset voltage to a useful voltage that depends on the lighting; and a phase of reading a voltage representative of the useful voltage, wherein the isolation of the photodiode from the read node at the end of the waiting phase comprises the steps of setting the transfer transistor to the on state, the reset transistor being off; turning off the transfer transistor; and setting the reset transistor to the on state.

According to an embodiment of the present invention, the step of setting the transfer transistor to the on state is preceded by a step of turning off the reset transistor, the transfer transistor being off.

According to an embodiment of the present invention, a turning-off of the transfer transistor is performed during the read phase preceding the waiting phase, the transfer transistor being maintained off at the beginning of the waiting phase.

According to an embodiment of the present invention, a turning-off of the transfer transistor is performed during the waiting phase before turning-off of the reset transistor.

According to an embodiment of the present invention, the reset transistor is turned on as soon as the read phase preceding the waiting phase is over, and is

maintained on at the beginning of the waiting phase.

According to an embodiment of the present invention, the step of turning off the reset transistor is carried out during the read phase preceding the waiting phase, the reset transistor being maintained off at the beginning of the waiting phase.

According to an embodiment of the present invention, the transfer transistor is temporarily turned on several times to discharge the photodiode at the end of the waiting phase, the reset transistor being maintained off.

The present invention also provides a device for controlling a photosensitive cell comprising a photodiode having its voltage varying according to the lighting, the photodiode being connected to a read node via a MOS transfer transistor, the read node being connected to a source of a reference voltage via a MOS reset transistor, a means for reading a voltage representative of the photodiode voltage, a means for isolating the photodiode from the reference voltage, and a timing means for delaying the photodiode isolation by the isolation means after reading of the representative voltage by the read means, wherein the isolation means comprises a means for temporarily turning on the transfer transistor while maintaining the reset transistor off.

According to an embodiment of the present invention, the MOS reset transistor and/or the MOS transfer transistor are shared between several photosensitive cells.

According to an embodiment of the present invention, the read means is shared between several photosensitive cells.

The foregoing object, features, and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

Brief Description Of The Drawings

Fig. 1, previously described, shows an electric diagram of a photosensitive cell;

Fig. 2, previously described, illustrates a conventional timing diagram of characteristic voltages of the circuit of Fig. 1;

Fig. 3 shows a partial simplified cross-section view of a portion of the circuit of Fig. 1 made in monolithic form;

Figs. 4A to 4H schematically show voltage levels in the structure of Fig. 3 at given times of the timing diagram of Fig. 2; and

Fig. 5 shows an example of a timing diagram of characteristic voltages according to the present invention of the circuit of Fig. 1.

Detailed Description

The present inventors have studied the variation of the characteristic voltages at the level of a photosensitive cell to reveal the phenomena that favor the charge return in a read cycle or before the beginning of an integration phase of a photosensitive cell.

Fig. 3 illustrates, in a partial simplified cross-section view, a conventional implementation in monolithic form of the assembly of photodiode D, transfer transistor M_4, and reset transistor M_1 of Fig. 1. These elements are formed in the same active area of a heavily-doped semiconductor substrate 1 of a first conductivity type, for example, type P (P^+). The substrate is connected to reference supply rail GND. The active area corresponds to a layer 3 of same conductivity type as underlying substrate 1, but more lightly doped, for example, an epitaxial layer. Above the surface of layer 3 are formed two insulated gate structures 4, 5, possibly provided with lateral spacers, respectively associated with transistors M_4 and M_1. To the left of gate 4, between gates 4, 5 and to the right of gate 5, are respectively present at the surface of layer 3 regions 6, 7, 8 of the opposite conductivity type, for example, N.

Region 7, intermediary between gates 4, 5, is heavily doped (N^+) and respectively forms the drain and the source of transistors M_4 and M_1. It is called hereafter the read region 7. Region 6 to the left of gate structure 4, which will be called the photodiode region hereafter, is formed on a much greater surface area than read region 7. It forms the source of transistor M_4 and forms with underlying layer 3 the junction of photodiode D. Region 8, to the right of gate 5, which will be called the supply region hereafter, forms the drain of transistor M_1. Gate 4, read region 7, gate 5, and supply region 8 are integral with connections (not shown) that enable putting in contact these regions respectively with transfer control signal T_X, the gate of transistor M_2 (node S), reset control signal RST, and supply rail Vdd. Photodiode D is of the so-called completely depleted type and comprises, at the surface of photodiode region 6, a P-type region 10, shallow and more heavily doped (P^+) than layer 3 and connected to the reference voltage

or to ground via layer 3 and substrate 1. The channel regions of transistors M_4 and M_1 are respectively designated with reference numerals 11 and 12.

Figs. 4A to 4H schematically illustrate the highest voltage levels in the different regions of Fig. 3 successively at successive times t_0 and t_6 of the timing diagram of Fig. 2.

At time t_0, at the beginning of a read cycle of the photosensitive cell, photodiode D has stored an amount of charges shown as a hatched area Q in Fig. 4A, delimited by a voltage V_D corresponding to the voltage in photodiode region 6 and voltage V_{DR} of photodiode D when it is completely discharged. Transfer control signal T_X is low. The voltage of channel region 11 of transistor M_4 is thus close to zero volt. Read region 7, of channel region 12 of transistor M_4, and of supply region 8, are at the voltage of power supply Vdd.

At time t_1, as shown in Fig. 4B, reset control signal RST is set to the low state. The voltage of channel region 12 of transistor M_1 is thus close to zero volt. Due to coupling phenomena between read region 7 and transistor M_1, the voltage of read region 7 becomes a voltage V_{RST} slightly smaller than the voltage of power supply Vdd.

At time t_2, as shown in Fig. 4C, transfer control signal T_X is set to a high state, sufficiently high for voltage V_C of channel region 11 to be greater than Vdd. The voltage of read region 7 increases to reach a voltage V_0 due to the coupling between transistor M_4 and read region 7. This enables increasing the electric field favoring the charge transfer from photodiode D to read node S. The charges stored at the level of photodiode D flow to read region 7 and raise the voltage of this region to value V_1. In the case where charge Q is relatively low, voltage V_1 may be greater than Vdd and greater than V_C. Hatched region Q' delimited by voltages V_0 and V_1 shows the charges stored at the level of read region 7.

At time t_3, as shown in Fig. 4D, transfer signal T_X is set to the low state. The voltage of channel region 11 of transistor M_4 then switches to zero. Since no charge is stored in channel region 11 for small charges Q, there then is no charge return to photodiode D. The coupling of the edge of transfer signal T_X brings voltage V_0'

substantially to voltage V_{RST} of Fig. 4B.

At time t_4, as shown in Fig. 4E, reset control signal RST is set to the low state. The voltage of channel region 12 of transistor M_1 thus increases to enable flowing of charges Q" stored at the level of read region 7 to supply region 8. The voltages of regions 7, 12, and 8 thus stabilize at the level of supply voltage Vdd.

At time t_5, as shown in Fig. 4F, after the end of the read cycle and before the beginning of the next integration phase, control signals T_X and RST have the same value as at time t_4. However, a certain amount of charges have been generated and stored at the level of diode D as shown by crossed-out region Q.

At time t_6, as shown in Fig. 4G, transfer control signal T_X is set to the high state. The charges stored at the level of photodiode D flow to supply region 8 and the voltages of regions 11, 7, 12, and 8 stabilize at value Vdd. Charges are then stored at the level of channel region 11 and are shown by hatched area Q" delimited by voltage Vdd and voltage V_C set by the value of the high state of transfer control signal T_X.

The present inventors have underlined, in Fig. 4G, that when signal T_X is set to the high state, no coupling occurs between transistor M_4 and read region 7. Indeed, transistor M_1 being off, read region 7 is not isolated from supply region 8 and is thus at low impedance.

At time t_7, as shown in Fig. 4H, transfer control signal T_X is set to the low state. Part of charges Q" stored at the level of channel region 11 in Fig. 4G then risk being sent back to the photodiode, as schematically illustrated by charge amount Q"'.

The present invention thus comprises providing a particular timing diagram of the control signals of a photosensitive cell before the beginning of a new integration phase to reduce the risk of charge return.

Fig. 5 shows two examples of implementation of a timing diagram according to the present invention. In the first example of implementation shown in full lines, reset signal RST is maintained on from the end of the read cycle and transfer control signal T_X is set to the high state little after the end of the read cycle. The control method provides, before the beginning of an integration phase T_{INT}, setting to the low state successively signal T_X and signal RST. Signal T_X is then set back to the high state for a short time,

then back to the low state. This then provides the favorable coupling illustrated in Fig. 4C between transistor M_4 and read region 7 due to the fact that said region is at high impedance upon setting to the high state of signal T_X since it is then isolated from supply region 8. The first falling edge of signal T_X is performed while signal RST is high, so that read region 7 is at low impedance and that there is no unfavorable coupling between transfer transistor M_4 and read region 7.

According to the present example of implementation, shown in dotted lines, signals RST and T_X are maintained low from the end of the preceding read cycle. The present invention provides setting to the high state signal RST for a short time, to completely discharge read node S and setting it back to the low state, than setting signal T_X to the high state for a short time, and setting it back to the low state while signal RST still is at the low state.

The present invention thus comprises, before starting a new integration period, performing a rising edge and a falling edge of the transfer control signal where read region 7 is at high impedance to benefit from a favorable coupling.

It should be noted that several successive pulses of transfer control signal T may be provided before the beginning of an integration period.

The control method according to the present invention enables obtaining, upon discharge of the photodiode before the beginning of an integration phase, a favorable coupling phenomenon which enables reducing the risk of charge return to the photodiode when the amount of charges stored in the photodiode is small. The occurrence of defects on an image formed based on the reading of the photosensitive cells is thus reduced, particularly for low lightings. This is particularly advantageous given the increased sensitivity of users to defects of images obtained under low lightings.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In particular, the present invention has been described in the context of a photosensitive cell with four MOS transistors (4T cell). It should be clear that the present invention finds an application for other types of photosensitive cells. It may be, for example, a photosensitive cell having one or several MOS transistors in common with one or several other photosensitive cells.

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is: